

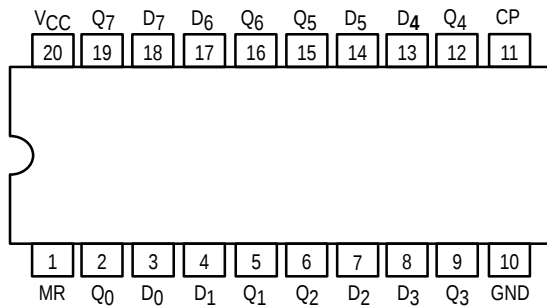


# OCTAL D FLIP-FLOP WITH CLEAR

The SN54/74LS273 is a high-speed 8-Bit Register. The register consists of eight D-Type Flip-Flops with a Common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch lead spacing.

- 8-Bit High Speed Register
- Parallel Register
- Common Clock and Master Reset
- Input Clamp Diodes Limit High-Speed Termination Effects

## CONNECTION DIAGRAM DIP (TOP VIEW)



## PIN NAMES

CP Clock (Active HIGH Going Edge) Input  
D<sub>0</sub>–D<sub>7</sub> Data Inputs  
MR Master Reset (Active LOW) Input  
Q<sub>0</sub>–Q<sub>7</sub> Register Outputs (Note b)

## LOADING (Note a)

|                                | HIGH     | LOW          |
|--------------------------------|----------|--------------|
| CP                             | 0.5 U.L. | 0.25 U.L.    |
| D <sub>0</sub> –D <sub>7</sub> | 0.5 U.L. | 0.25 U.L.    |
| MR                             | 0.5 U.L. | 0.25 U.L.    |
| Q <sub>0</sub> –Q <sub>7</sub> | 10 U.L.  | 5 (2.5) U.L. |

## NOTES:

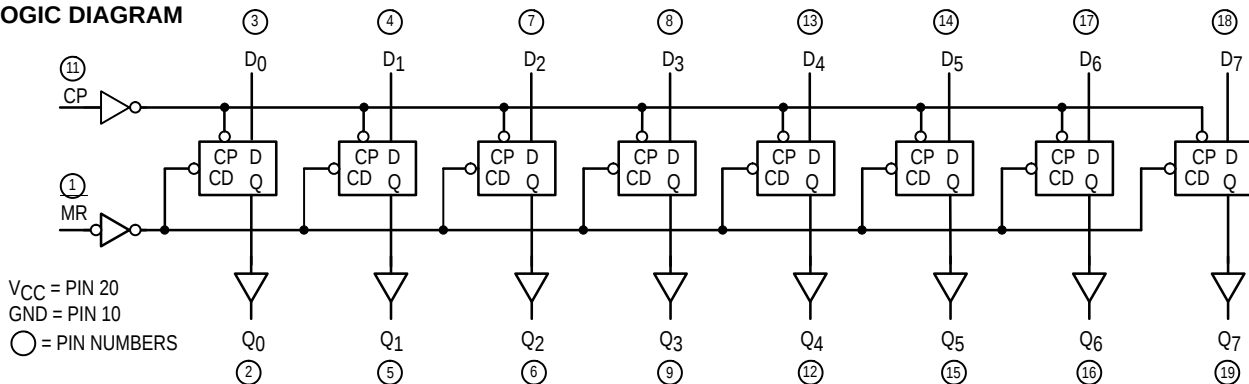
- a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.  
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

## TRUTH TABLE

| MR | CP | D <sub>x</sub> | Q <sub>x</sub> |
|----|----|----------------|----------------|
| L  | X  | X              | L              |
| H  |    | H              | H              |
| H  |    | L              | L              |

H = HIGH Logic Level  
L = LOW Logic Level  
X = Immaterial

## LOGIC DIAGRAM

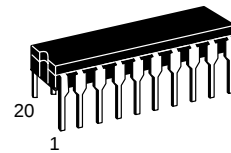


V<sub>CC</sub> = PIN 20  
GND = PIN 10  
○ = PIN NUMBERS

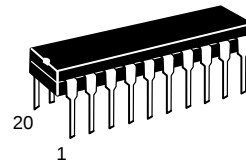
**SN54/74LS273**

**OCTAL D FLIP-FLOP  
WITH CLEAR**

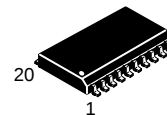
**LOW POWER SCHOTTKY**



**J SUFFIX  
CERAMIC  
CASE 732-03**



**N SUFFIX  
PLASTIC  
CASE 738-03**



**DW SUFFIX  
SOIC  
CASE 751D-03**

## ORDERING INFORMATION

SN54LSXXXJ Ceramic  
SN74LSXXXN Plastic  
SN74LSXXXDW SOIC

# SN54/74LS273

## FUNCTIONAL DESCRIPTION

The SN54/74LS273 is an 8-Bit Parallel Register with a common Clock and common Master Reset.

When the MR input is LOW, the Q outputs are LOW,

independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

## GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |          | Min         | Typ        | Max         | Unit |
|-----------------|-------------------------------------|----------|-------------|------------|-------------|------|
| V <sub>CC</sub> | Supply Voltage                      | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 54<br>74 | −55<br>0    | 25<br>25   | 125<br>70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 54, 74   |             |            | −0.4        | mA   |
| I <sub>OL</sub> | Output Current — Low                | 54<br>74 |             |            | 4.0<br>8.0  | mA   |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter                      |        | Limits |       |      | Unit | Test Conditions                                                                                                    |
|-----------------|--------------------------------|--------|--------|-------|------|------|--------------------------------------------------------------------------------------------------------------------|
|                 |                                |        | Min    | Typ   | Max  |      |                                                                                                                    |
| V <sub>IH</sub> | Input HIGH Voltage             |        | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs                                                                       |
| V <sub>IL</sub> | Input LOW Voltage              | 54     |        |       | 0.7  | V    | Guaranteed Input LOW Voltage for All Inputs                                                                        |
|                 |                                | 74     |        |       | 0.8  |      |                                                                                                                    |
| V <sub>IK</sub> | Input Clamp Diode Voltage      |        |        | −0.65 | −1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = −18 mA                                                                    |
| V <sub>OH</sub> | Output HIGH Voltage            | 54     | 2.5    | 3.5   |      | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table |
|                 |                                | 74     | 2.7    | 3.5   |      | V    |                                                                                                                    |
| V <sub>OL</sub> | Output LOW Voltage             | 54, 74 |        | 0.25  | 0.4  | V    | I <sub>OL</sub> = 4.0 mA                                                                                           |
|                 |                                | 74     |        | 0.35  | 0.5  | V    | I <sub>OL</sub> = 8.0 mA                                                                                           |
| I <sub>IH</sub> | Input HIGH Current             |        |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V                                                                     |
|                 |                                |        |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V                                                                     |
| I <sub>IL</sub> | Input LOW Current              |        |        |       | −0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V                                                                     |
| I <sub>OS</sub> | Short Circuit Current (Note 1) |        | −20    |       | −100 | mA   | V <sub>CC</sub> = MAX                                                                                              |
| I <sub>CC</sub> | Power Supply Current           |        |        |       | 27   | mA   | V <sub>CC</sub> = MAX                                                                                              |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

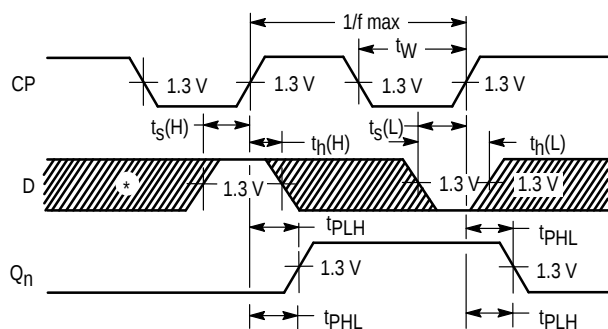
| Symbol                               | Parameter                          | Limits |          |          | Unit | Test Conditions |
|--------------------------------------|------------------------------------|--------|----------|----------|------|-----------------|
|                                      |                                    | Min    | Typ      | Max      |      |                 |
| f <sub>MAX</sub>                     | Maximum Input Clock Frequency      | 30     | 40       |          | MHz  | Figure 1        |
| t <sub>PHL</sub>                     | Propagation Delay, MR to Q Output  |        | 18       | 27       | ns   | Figure 2        |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay, Clock to Output |        | 17<br>18 | 27<br>27 | ns   | Figure 1        |

# SN54/74LS273

## AC SETUP REQUIREMENTS ( $T_A = 25^\circ\text{C}$ , $V_{CC} = 5.0\text{ V}$ )

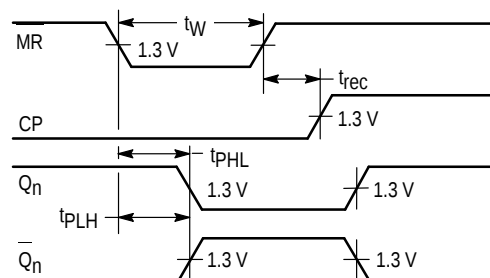
| Symbol    | Parameter                   | Limits |     |     | Unit | Test Conditions |
|-----------|-----------------------------|--------|-----|-----|------|-----------------|
|           |                             | Min    | Typ | Max |      |                 |
| $t_W$     | Pulse Width, Clock or Clear | 20     |     |     | ns   | Figure 1        |
| $t_S$     | Data Setup Time             | 20     |     |     | ns   | Figure 1        |
| $t_H$     | Hold Time                   | 5.0    |     |     | ns   | Figure 1        |
| $t_{rec}$ | Recovery Time               | 25     |     |     | ns   | Figure 2        |

## AC WAVEFORMS



\*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Figure 1. Clock to Output Delays, Clock Pulse Width, Frequency, Setup and Hold Times Data to Clock**



**Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time**

## DEFINITION OF TERMS

**SETUP TIME ( $t_S$ )** — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

**HOLD TIME ( $t_H$ )** — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued

recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

**RECOVERY TIME ( $t_{rec}$ )** — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH data to the Q outputs.