



**National  
Semiconductor**

## MM2114/MM2114L Family 4096-Bit (1024 × 4) Static RAMs

| Maximum Access/Current               | MM2114-15L | MM2114-2L | MM2114-25L | MM2114-3L | MM2114-L | MM2114-15 | MM2114-2 | MM2114-25 | MM2114-3 | MM2114 |
|--------------------------------------|------------|-----------|------------|-----------|----------|-----------|----------|-----------|----------|--------|
| Access (TAVQV—ns)                    | 150        | 200       | 250        | 300       | 450      | 150       | 200      | 250       | 300      | 450    |
| Active Current (I <sub>CC</sub> —mA) | 70         | 70        | 70         | 70        | 70       | 100       | 100      | 100       | 100      | 100    |

### General Description

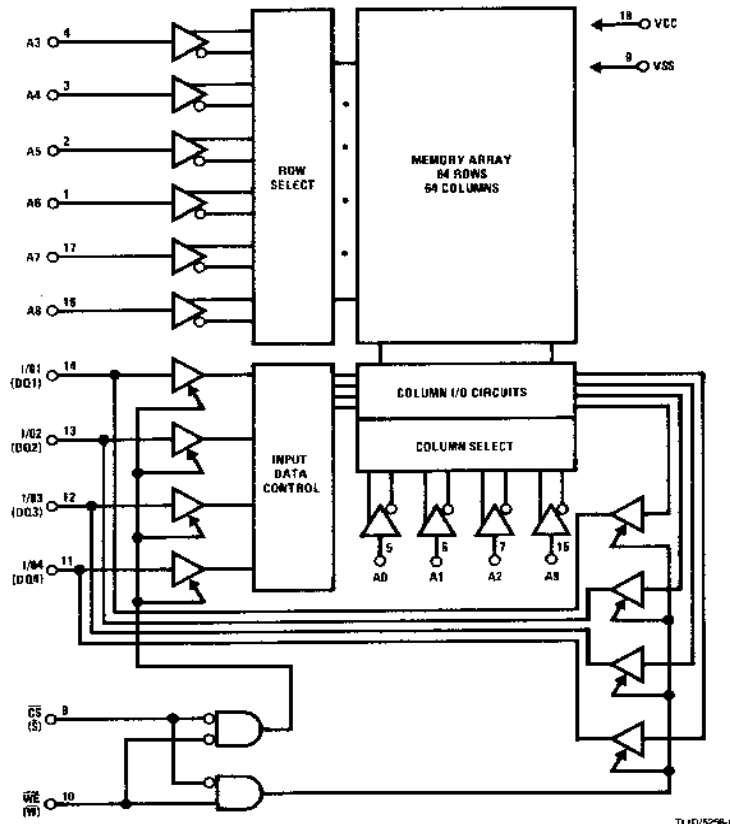
The MM2114 family of 1024-word by 4-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The separate chip select input ( $\overline{CS}$ ) allows easy memory expansion by OR-tying individual devices to a data bus.

### Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 150 ns access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Standard 18-pin dual-in-line package
- Available with MIL-STD-883 class B screening

### Block Diagram\*



\* Symbols in parentheses are proposed industry standard.

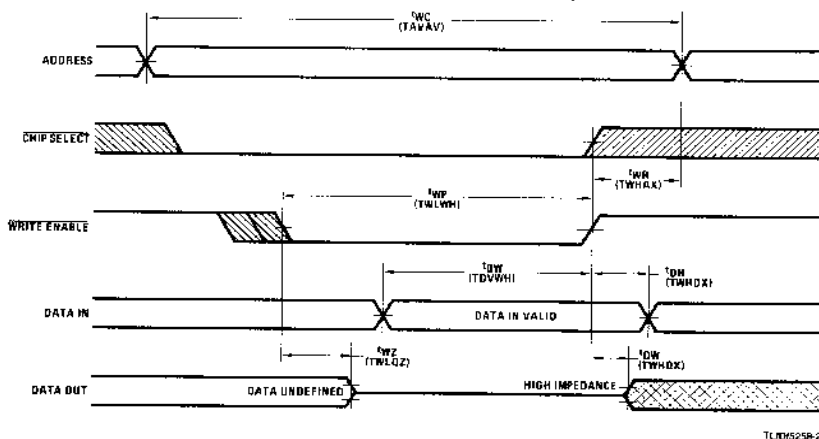
# Write Cycle AC Electrical Characteristics (Note 3) $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{V} \pm 5\%$

| Symbol    |          | Parameter                                     | MM2114-15<br>MM2114-15L |     | MM2114-2<br>MM2114-2L |     | MM2114-25<br>MM2114-25L |     | MM2114-3<br>MM2114-3L |     | MM2114<br>MM2114-L |     | Units |
|-----------|----------|-----------------------------------------------|-------------------------|-----|-----------------------|-----|-------------------------|-----|-----------------------|-----|--------------------|-----|-------|
| Alternate | Standard |                                               | Min                     | Max | Min                   | Max | Min                     | Max | Min                   | Max | Min                | Max |       |
| $t_{WC}$  | TAVAV    | Write Cycle Time                              | 150                     |     | 200                   |     | 250                     |     | 300                   |     | 450                |     | ns    |
| $t_{WP}$  | TWLWH    | Write Pulse Width                             | 90                      |     | 100                   |     | 125                     |     | 150                   |     | 200                |     | ns    |
| $t_{WR}$  | TWHAX    | Write Recovery Time                           | 0                       |     | 0                     |     | 0                       |     | 0                     |     | 0                  |     | ns    |
| $t_{DW}$  | TDVWH    | Data Set-Up Time                              | 90                      |     | 100                   |     | 125                     |     | 150                   |     | 200                |     | ns    |
| $t_{DH}$  | TWHDX    | Data Hold Time                                | 0                       |     | 0                     |     | 0                       |     | 0                     |     | 0                  |     | ns    |
| $t_{WZ}$  | TWLQZ    | Write Enable to Output TRI-STATE (Note 5)     | 0                       | 40  | 0                     | 40  | 0                       | 60  | 0                     | 80  | 0                  | 100 | ns    |
| $t_{OW}$  | TWHQX    | Output Active from End of Write (WE) (Note 5) |                         | 80  |                       | 80  |                         | 90  |                       | 100 |                    | 120 | ns    |

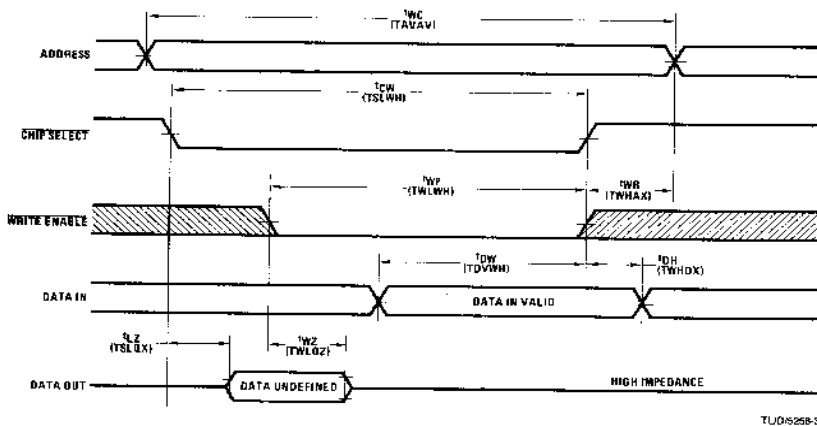
\* Symbols in parentheses are proposed industry standard.

## Write Cycle Waveforms\* (Note 4)

Write Cycle 1 (Write Enable Limited)



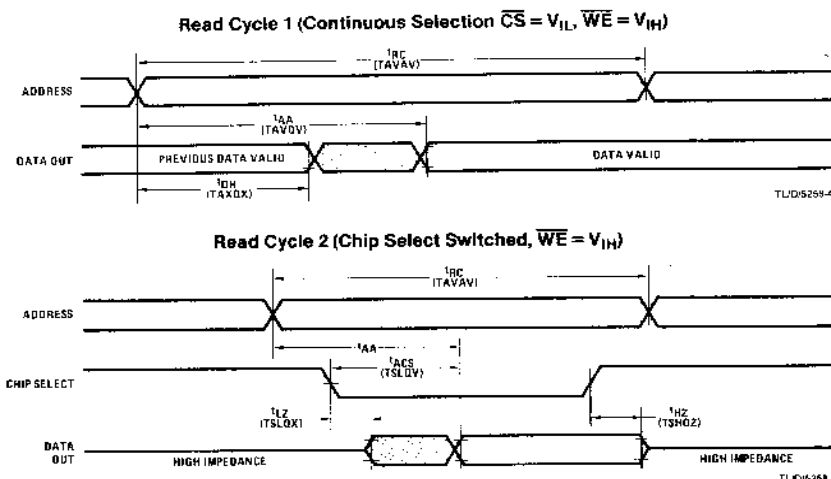
Write Cycle 2 (Chip Select Limited)



# Read Cycle AC Electrical Characteristics $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{V} \pm 5\%$

| Symbol    |          | Parameter                                    | MM2114-15<br>MM2114-15L |     | MM2114-2<br>MM2114-2L |     | MM2114-25<br>MM2114-25L |     | MM2114-3<br>MM2114-3L |     | MM2114<br>MM2114-L |     | Units |
|-----------|----------|----------------------------------------------|-------------------------|-----|-----------------------|-----|-------------------------|-----|-----------------------|-----|--------------------|-----|-------|
| Alternate | Standard |                                              | Min                     | Max | Min                   | Max | Min                     | Max | Min                   | Max | Min                | Max |       |
| $t_{RC}$  | TAVAV    | Read Cycle Time ( $\overline{WE} = V_{IH}$ ) | 150                     |     | 200                   |     | 250                     |     | 300                   |     | 450                |     | ns    |
| $t_{AA}$  | TAVQV    | Address Access Time                          |                         | 150 |                       | 200 |                         | 250 |                       | 300 |                    | 450 | ns    |
| $t_{ACS}$ | TSLQV    | Chip Select Access Time                      |                         | 70  |                       | 70  |                         | 90  |                       | 100 |                    | 120 | ns    |
| $t_{LZ}$  | TSLQX    | Chip Select to Output Active (Note 5)        | 20                      |     | 20                    |     | 20                      |     | 20                    |     | 20                 |     | ns    |
| $t_{HZ}$  | TSHQZ    | Chip Deselect to Output TRI-STATE (Note 5)   | 0                       | 40  | 0                     | 40  | 0                       | 60  | 0                     | 80  | 0                  | 100 | ns    |
| $t_{OH}$  | TAXQX    | Output Hold from Address Change              | 15                      |     | 10                    |     | 10                      |     | 10                    |     | 10                 |     | ns    |

## Read Cycle Waveforms\*



Note 3: A write occurs during the coincidence low of  $\overline{CS}$  and  $\overline{WE}$ .

Note 4: The output remains TRI-STATE if the  $\overline{CS}$  and  $\overline{WE}$  go high simultaneously.  $\overline{WE}$  or  $\overline{CS}$  or both must be high during the address transitions.

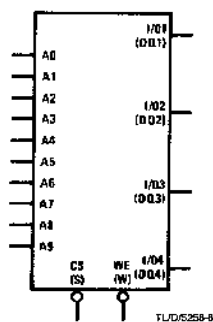
Note 5: Measured  $\pm 50\text{ mV}$  from steady state voltage. This parameter is sampled and not 100% tested.

## DC Electrical Characteristics $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{CC} = 5\text{V} \pm 5\%$

| Symbol   | Parameter                              | Conditions                                                        | MM2114, MM2114-15,<br>MM2114-2, MM2114-25,<br>MM2114-3 |          | MM2114-L, MM2114-15L,<br>MM2114-2L, MM2114-25L,<br>MM2114-3L |          | Units         |
|----------|----------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------|----------|--------------------------------------------------------------|----------|---------------|
|          |                                        |                                                                   | Min                                                    | Max      | Min                                                          | Max      |               |
| $I_{LI}$ | Input Load Current<br>(All Input Pins) | $V_{IN} = 0\text{V}$ to $5.25\text{V}$                            | -10                                                    | 10       | -10                                                          | 10       | $\mu\text{A}$ |
| $I_{LO}$ | Output Leakage Current                 | $\overline{CS} = V_{IH}$ , $V_{OUT} = 0.4\text{V}$ to $4\text{V}$ | -10                                                    | 10       | -10                                                          | 10       | $\mu\text{A}$ |
| $V_{IL}$ | Input Low Voltage                      |                                                                   | -0.5                                                   | 0.8      | -0.5                                                         | 0.8      | V             |
| $V_{IH}$ | Input High Voltage                     |                                                                   | 2.0                                                    | $V_{CC}$ | 2.0                                                          | $V_{CC}$ | V             |
| $V_{OL}$ | Output Low Voltage                     | $I_{OL} = 2.1\text{ mA}$                                          |                                                        | 0.4      |                                                              | 0.4      | V             |
| $V_{OH}$ | Output High Voltage                    | $I_{OH} = -1.0\text{ mA}$                                         | 2.4                                                    |          | 2.4                                                          |          | V             |
| $I_{CC}$ | Power Supply Current                   | $V_{IN} = 5.25\text{V}$ , $T_A = 0^\circ\text{C}$<br>Outputs Open |                                                        | 100      |                                                              | 70       | mA            |

\* The symbols in parentheses are proposed industry standard.

## Logic Symbol\*

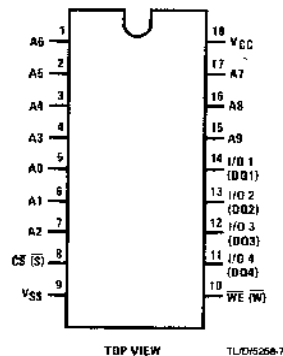


## Pin Names\*

|                     |                   |
|---------------------|-------------------|
| A0-A9               | Address Inputs    |
| WE (W)              | Write Enable      |
| CS (S)              | Chip Select       |
| I/O1-I/O4 (DQ1-DQ4) | Data Input/Output |

## Connection Diagram\*

## Dual-In-Line Package



Order Number MM2114N-15L, MM2114N-15,  
MM2114N-2L, MM2114N-2, MM2114N-3L,  
MM2114N-3, MM2114N-1 or MM2114N  
NS Package Number N18A

## Absolute Maximum Ratings

|                                          |                   |
|------------------------------------------|-------------------|
| Voltage at Any Pin                       | - 0.5V to + 7V    |
| Storage Temperature                      | - 65°C to - 150°C |
| Power Dissipation                        | 1W                |
| Lead Temperature (Soldering, 10 seconds) | 300°C             |

## Operating Conditions

|                                       | Min  | Max  | Units |
|---------------------------------------|------|------|-------|
| Supply Voltage (V <sub>CC</sub> )     | 4.75 | 5.25 | V     |
| Ambient Temperature (T <sub>A</sub> ) | 0    | + 70 | °C    |

Capacitance T<sub>A</sub> = 25°C, f = 1 MHz (Note 1)

| Symbol                       | Parameter          | Conditions                      | MM2114, MM2114-15,<br>MM2114-2, MM2114-25,<br>MM2114-3 |     | MM2114-L, MM2114-15L,<br>MM2114-2L, MM2114-25L,<br>MM2114-3L |     | Units |
|------------------------------|--------------------|---------------------------------|--------------------------------------------------------|-----|--------------------------------------------------------------|-----|-------|
|                              |                    |                                 | Min                                                    | Max | Min                                                          | Max |       |
| C <sub>IN</sub>              | Input Capacitance  | All Inputs V <sub>IN</sub> = 0V |                                                        | 5   |                                                              | 5   | pF    |
| C <sub>OUT</sub><br>(Note 2) | Output Capacitance | V <sub>O</sub> = 0V             |                                                        | 5   |                                                              | 5   | pF    |

Note 1: This parameter is guaranteed by periodic testing.

Note 2: C<sub>OUT</sub> is max 10 pF for (J) package.

## AC Test Conditions

|                           |          |                                  |                          |
|---------------------------|----------|----------------------------------|--------------------------|
| Input Pulse Levels        | 0V to 3V | Output Load and<br>Timing Levels | 0.8V @ 2.1 mA + 100 pF   |
| Input Rise and Fall Times | ≤ 10 ns  |                                  | 2.0V @ - 1.0 mA + 100 pF |
| Input Timing Level        | 1.5V     |                                  |                          |

\*Symbols in parentheses are proposed industry standard.