MOTOROLA

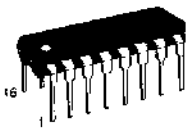
MC14529B

DUAL 4-CHANNEL ANALOG DATA SELECTOR

The MC14529B analog data selector is a dual 4-channel or single 8-channel device depending on the input coding. The device is suitable for digital as well as analog application, including various one-of-four and one-of-eight data selector functions. Since the device has bidirectional analog characteristics it can also be used as a dual binary to 1-of-4 or a binary to 1-of-8 decoder.

- Data Paths Are Bidirectional
- 3-State Outputs
- Linear "On" Resistance
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load over the Rated Temperature Range.

L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP Plastic
MC14XXXBCL Ceramic
MC14XXXBD SOIC

T_A = −55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

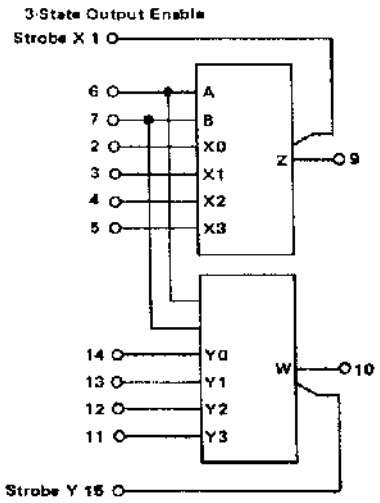
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: −7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: −12 mW/°C From 100°C To 125°C

TRUTH TABLE

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance		

X = Don't Care

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}. Switch I/O: $V_{SS} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq 500$ mV**	— — —	1.0 1.0 2.0	— — —	0.005 0.010 0.015	1.0 1.0 2.0	— — —	60 60 120	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz)f + I_{DD} (0.20 μA/kHz)f + I_{DD} (0.36 μA/kHz)f + I_{DD}				μA
CONTROL INPUTS — INHIBIT, A, B (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High-Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — W, Z (Voltages Referenced to V_{EE})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 5)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	10 15	$\Delta V_{switch} \leq 500$ mV**, $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	— —	400 240	— —	120 80	480 270	— —	560 350	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	10 15		— —	— —	— —	15 10	— —	— —	— —	Ω
Off-Channel Leakage Current (Figure 10)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	8.0	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	Inhibit = V_{DD}	—	—	—	20	—	—	—	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	— —	— —	— —	0.15 0.47	— —	— —	— —	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

SWITCHING CHARACTERISTICS (T_A = 25°C)

Characteristic	Figure	Symbol	V_{SS}	V_{DD}	Min	Typ #	Max	Unit
V_{in} to V_{out} Propagation Delay Time (C_L = 50 pF, R_L = 1.0 kΩ)	7	t_{PLH}, t_{PHL}	0.0	5.0 10 15	— — —	20 10 8.0	40 20 15	ns
Propagation Delay Time, Control to Output, V_{in} = V_{DD} or V_{SS} (C_L = 50 pF, R_L = 1.0 kΩ)	8	t_{PLZ}, t_{PZL}, t_{PHZ}, t_{PZH}	0.0	5.0 10 15	— — —	140 70 60	400 160 120	ns
Crosstalk, Control to Output (C_L = 50 pF, R_L = 1.0 kΩ R_{out} = 10 kΩ)	9	—	0.0	5.0 10 15	— — —	5.0 5.0 5.0	— — —	mV
Control Input Pulse Frequency (C_L = 50 pF, R_L = 1.0 kΩ)	10	f_{in}	0.0	5.0 10 15	— — —	5.0 10 12	2.5 6.2 8.3	MHz
Noise Voltage (f = 100 Hz)	11,12	—	0.0	5.0 10 15 5.0 10 15	— — — — — —	24 25 30 12 12 15	— — — — — —	$\frac{nV}{\sqrt{cycle}}$
Sine Wave Distortion (V_{in} = 1.77 Vdc RMS Centered @ 0.0 Vdc, R_L = 10 kΩ, f = 1.0 kHz)	—	—	−5.0	5.0	—	0.36	—	%
Off-Channel Leakage Current (V_{in} = +5.0 Vdc, V_{out} = −5.0 Vdc) (V_{in} = −5.0 Vdc, V_{out} = +5.0 Vdc) (V_{in} = +7.5 Vdc, V_{out} = −7.5 Vdc) (V_{in} = −7.5 Vdc, V_{out} = +7.5 Vdc)	—	I_{off}	 −5.0 −5.0 −7.5 −7.5	 5.0 5.0 7.5 7.5	 — — — —	 ±0.001 ±0.001 ±0.0015 ±0.0015	 ±125 ±125 ±250 ±250	nA
Insertion Loss (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc, f = 1.0 MHz) $l_{loss} = 20 \log_{10} \frac{V_{out}}{V_{in}}$ (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	13	—	−5.0	5.0	 — — — —	 2.0 0.8 0.25 0.01	 — — — —	dB
Bandwidth (−3 dB) (V_{in} = 1.77 Vdc RMS centered @ 0.0 Vdc) (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	—	BW	−5.0	5.0	 — — — —	 35 28 27 26	 — — — —	MHz
Feedthrough and Crosstalk $20 \log_{10} \frac{V_{out}}{V_{in}} = -50$ dB (R_L = 1.0 kΩ) (R_L = 10 kΩ) (R_L = 100 kΩ) (R_L = 1.0 MΩ)	—	—	−5.0	5.0	 — — — —	 850 100 12 1.5	 — — — —	MHz

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FIGURE 1 - OUTPUT VOLTAGE TEST CIRCUIT

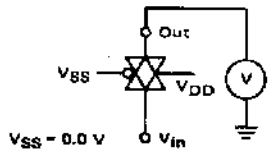
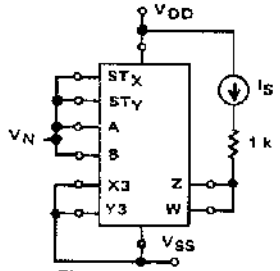


FIGURE 2 – NOISE IMMUNITY TEST CIRCUIT



Pins 2, 3, 4, 12, 13 and 14 are left open.

V_{IL}: V_C is raised from V_{SS} until $V_C = V_{IL}$ at $V_C = V_{IL}$: $I_S = \pm 10\ \mu A$ with $V_{in} = V_{SS}$, $V_{out} = V_{DD}$ or $V_{in} = V_{DD}$, $V_{out} = V_{SS}$.

V_{IH}: When $V_C = V_{IH}$ to V_{DD}, the switch is ON and the R_{ON} specifications are met.

FIGURE 3 – QUIESCENT POWER DISSIPATION TEST CIRCUIT

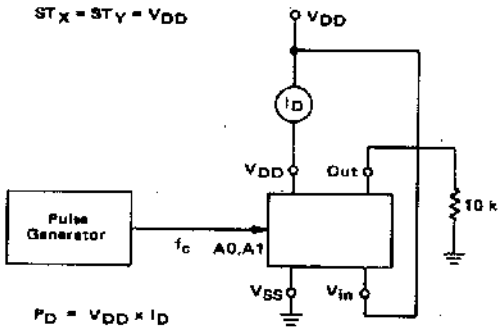
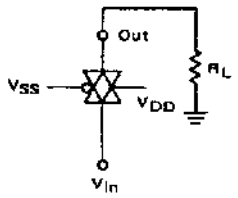


FIGURE 4 – R_{ON} CHARACTERISTICS TEST CIRCUIT



TYPICAL R_{ON} versus INPUT VOLTAGE

FIGURE 5

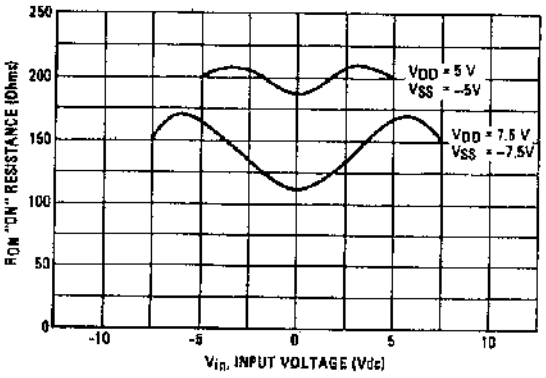


FIGURE 6

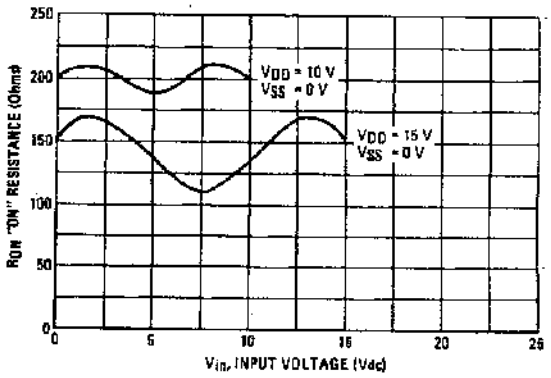


FIGURE 7 – PROPAGATION DELAY TEST CIRCUIT AND WAVEFORMS

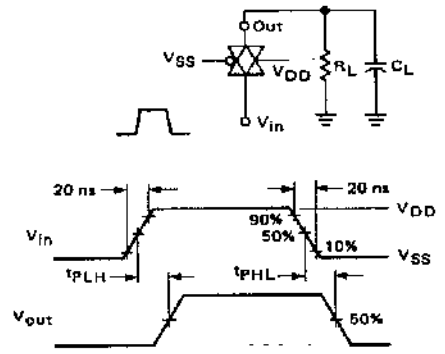


FIGURE 8 – TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

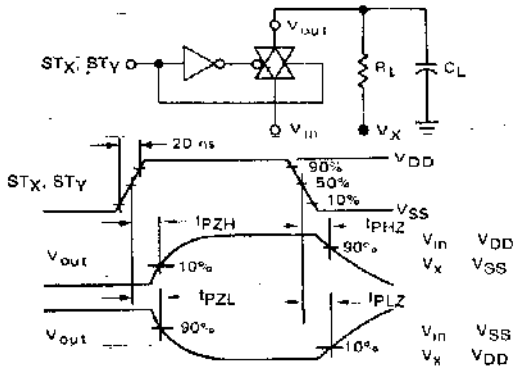


FIGURE 9 – CROSSTALK TEST CIRCUIT

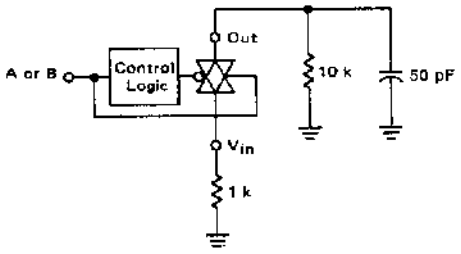


FIGURE 10 – FREQUENCY RESPONSE TEST CIRCUIT

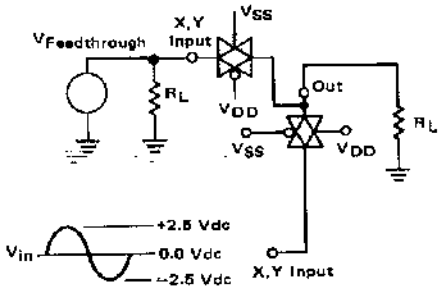


FIGURE 11 – NOISE VOLTAGE TEST CIRCUIT

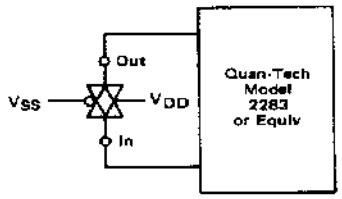


FIGURE 12 – TYPICAL NOISE CHARACTERISTICS

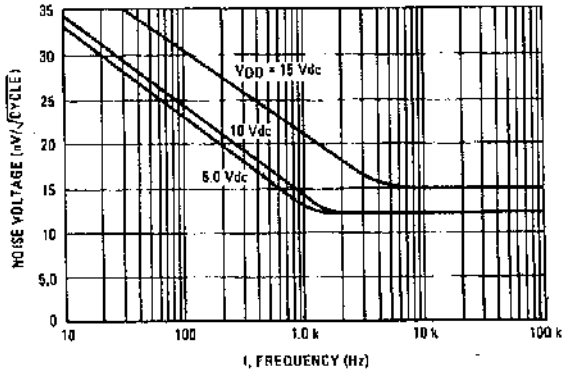
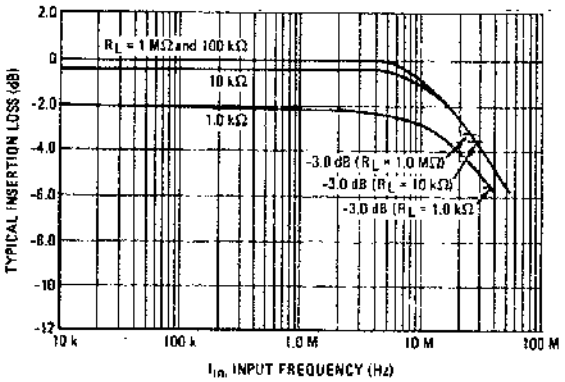
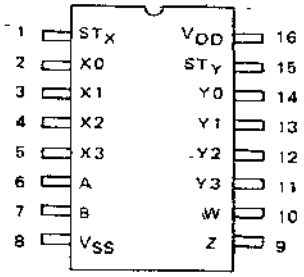


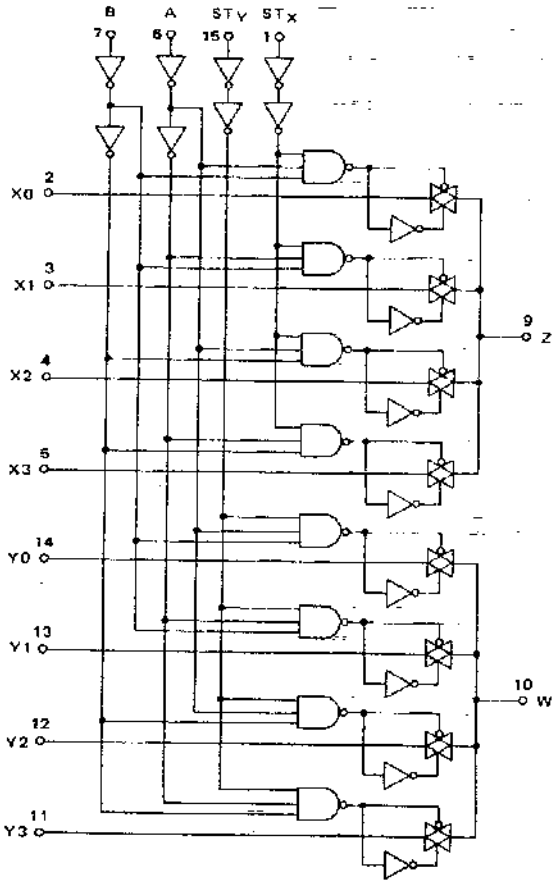
FIGURE 13 – TYPICAL INSERTION LOSS/BANDWIDTH CHARACTERISTICS



PIN ASSIGNMENT



LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8