

U.H.F. LINEAR POWER TRANSISTOR

N-P-N multi-emitter silicon planar epitaxial transistor primarily for use in linear u.h.f. amplifiers for television transposers and transmitters.

Features:

- guaranteed low intermodulation figures;
- gold metallization ensures excellent reliability.

The transistor has a $\frac{1}{4}$ " capstan envelope with a moulded cap. All leads are isolated from the stud.

QUICK REFERENCE DATA

R.F. performance in linear amplifier

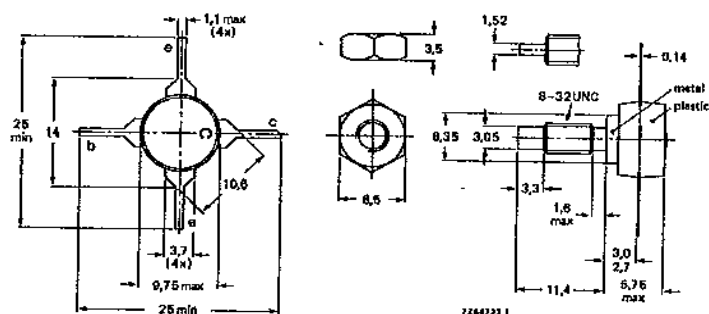
mode of operation	f_{vision} MHz	V_{CE} V	I_{C} mA	T_{h} °C	d_{im} dB	$P_{\text{o sync}}$ W	G_{p} dB
class-A	860	25	500	25	-60	> 1,0	> 5,5
class-A	860	25	500	25	-60	typ. 1,1	typ. 6,5

* Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), zero dB corresponds to peak sync level.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-48/3.



Torque on nut: min. 0,75 Nm
(7,5 kg cm)
max. 0,85 Nm
(8,5 kg cm)

Diameter of clearance hole in heatsink: max. 4,2 mm.
Mounting hole to have no burrs at either end.
De-burring must leave surface flat; do not chamfer or countersink either end of hole.

When locking is required an adhesive is preferred instead of a lock washer.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

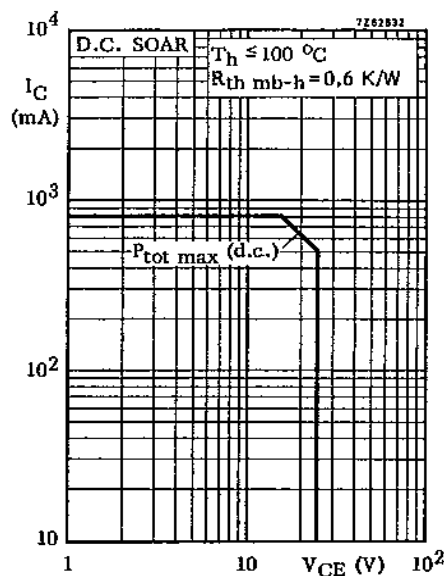
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RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Collector-base voltage (open emitter; peak value)	V_{CBOM}	max.	40	V
Collector-emitter voltage ($R_{BE} = 10 \Omega$; peak value)	V_{CERM}	max.	40	V
Collector-emitter voltage (open base)	V_{CEO}	max.	27	V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5	V
Collector current (d.c.)	I_C	max.	0,8	A
Collector current (peak value) $f > 1$ MHz	I_{CM}	max.	2	A
Total power dissipation up to $T_h = 100^\circ\text{C}$	P_{tot}	max.	12,5	W



Storage temperature	T_{stg}	-65 to +200	$^\circ\text{C}$
Junction temperature	T_j	max. 200	$^\circ\text{C}$

THERMAL RESISTANCE

From junction to mounting base	$R_{th j-mb}$	=	7,5	K/W
From mounting base to heatsink	$R_{th mb-h}$	=	0,6	K/W

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CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

Collector cut-off current

$I_E = 0; V_{CB} = 20\text{ V}$	I_{CBO}	<	200	μA
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Breakdown voltages

Collector-base voltage

open emitter; $I_C = 2\text{ mA}$	$V_{(BR)CBO}$	>	40	V
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Collector-emitter voltage

$R_{BE} = 10\ \Omega; I_C = 10\text{ mA}$	$V_{(BR)CER}$	>	40	V
open base; $I_C = 10\text{ mA}$	$V_{(BR)CEO}$	>	27	V

Emitter-base voltage

open collector; $I_E = 2\text{ mA}$	$V_{(BR)EBO}$	>	3, 5	V
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Saturation voltage

$I_C = 400\text{ mA}; I_B = 40\text{ mA}$	V_{CEsat}	<	0, 75	V
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D. C. current gain

$I_C = 400\text{ mA}; V_{CE} = 20\text{ V}$	h_{FE}	>	30	
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$I_C = 800\text{ mA}; V_{CE} = 20\text{ V}$	h_{FE}	>	20	
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Transition frequency

$I_C = 400\text{ mA}; V_{CE} = 20\text{ V}$	f_T	>	1, 2	GHz
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$I_C = 700\text{ mA}; V_{CE} = 20\text{ V}$	f_T	>	1, 0	GHz
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Collector capacitance at $f = 1\text{ MHz}$

$I_E = I_C = 0; V_{CB} = 20\text{ V}$	C_c	<	20	pF
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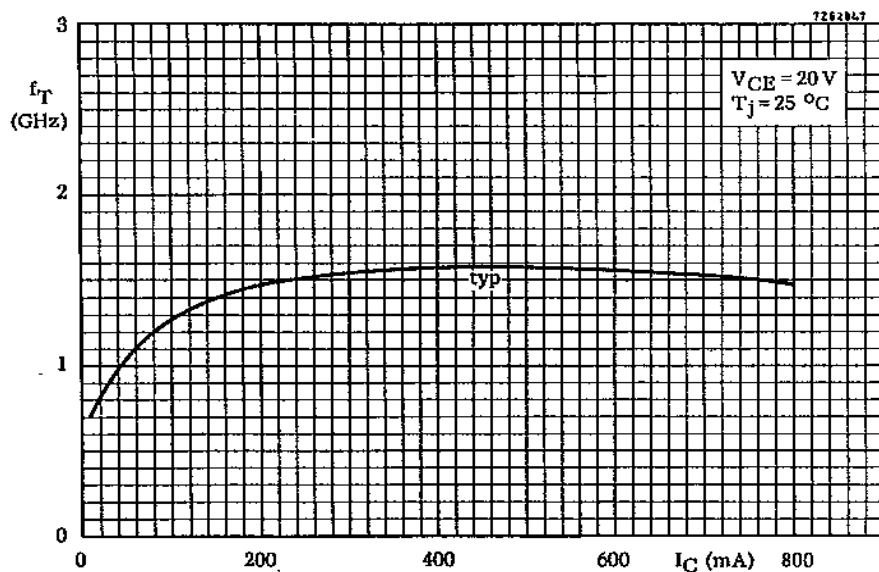
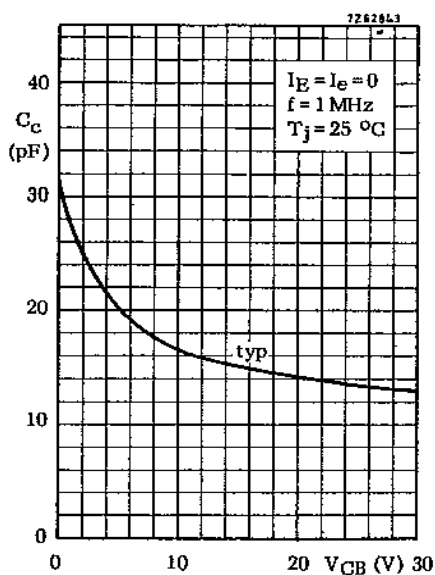
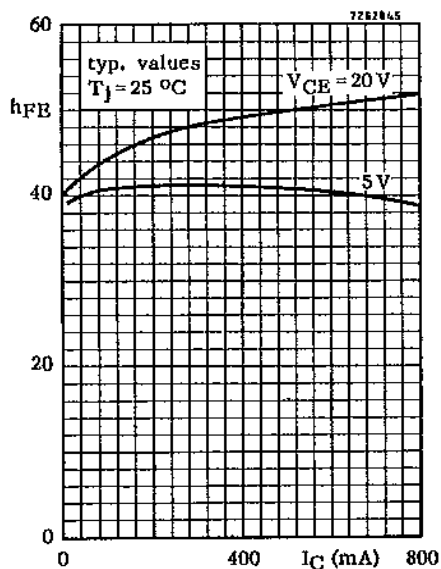
Feedback capacitance at $f = 1\text{ MHz}$

$I_C = 20\text{ mA}; V_{CE} = 20\text{ V}; T_{mb} = 25^\circ\text{C}$	C_{re}	typ.	7	pF
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Collector-stud capacitance

	C_{cs}	typ.	2	pF
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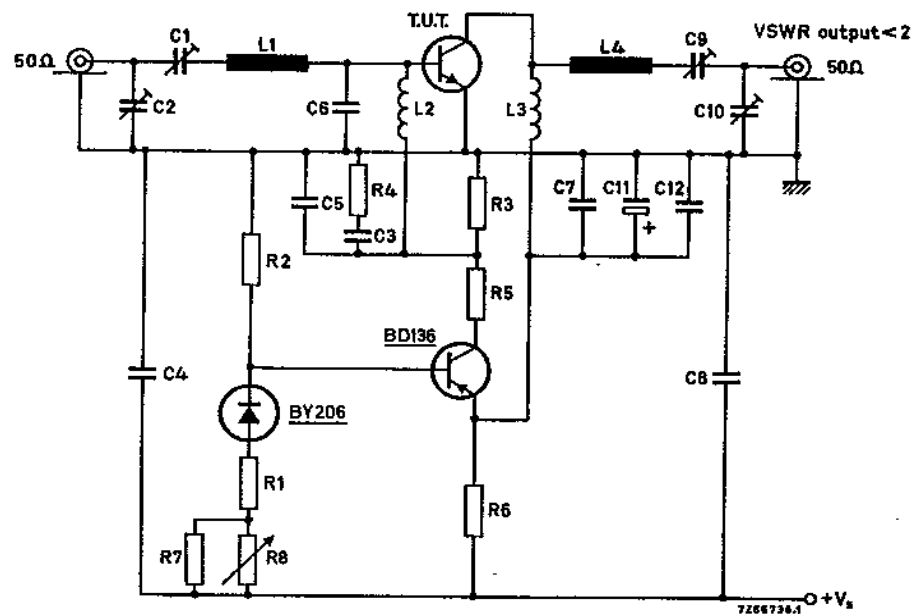
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APPLICATION INFORMATION

d _{im} (dB) *)	f _{vision} (MHz)	V _{CE} (V)	I _C (mA)	G _p (dB)	P _{o sync} (W) *)	T _h (°C)
-60	860	25	500	> 5,5	> 1,0	25
-60	860	25	500	typ. 6,5	typ. 1,1	25

*) Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), zero dB corresponds to peak sync level.

Test circuit at f_{vision} = 860 MHz



List of components: (see also page 6)

C1 = C2 = C10 = 2 to 9 pF film dielectric trimmers

C3 = C4 = C12 = 100 nF polyester capacitors

C5 = C7 = C8 = 100 pF feed-through capacitors

C6 = 2 x 2,7 pF in parallel, chip capacitors

C9 = 2 to 18 pF film dielectric trimmer

C11 = 10 μF/40 V solid aluminium electrolytic capacitor

R1 = 220 Ω

R5 = 470 Ω (1 W)

R2 = 4,7 kΩ

R6 = 3 x 22 Ω in parallel; (1 W)

R3 = 100 Ω

R7 = 12 kΩ

R4 = 10 Ω

R8 = 1 kΩ

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APPLICATION INFORMATION (continued)**List of components: (continued)**

L1 = stripline (14,8 mm x 4,3 mm)

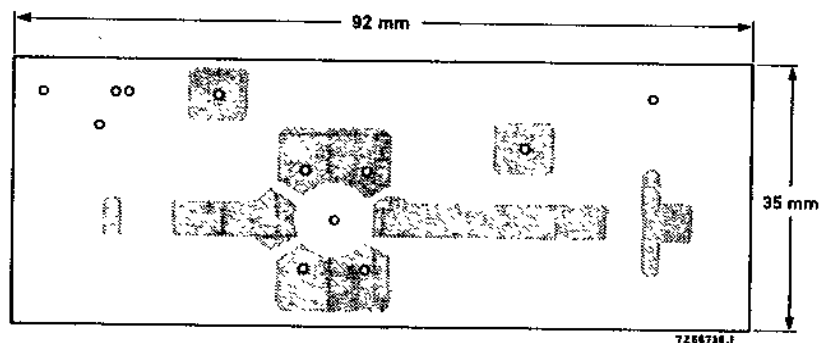
L2 = 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm

L3 = 2 turns Cu wire (1 mm); winding pitch 1,5 mm; int. dia. 4,5 mm; leads 2 x 5 mm

L4 = stripline (29,5 mm x 4,3 mm)

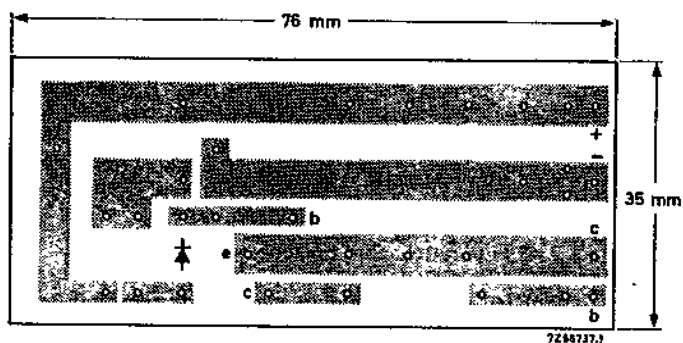
L1 and L4 are striplines on a double Cu-clad print plate with PTFE fibre-glass dielectric ($\epsilon_r = 2,74$); thickness 1,45 mm.

Layout of printed-circuit board for 860 MHz test circuit.



The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets.

Layout of printed board bias circuit.



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