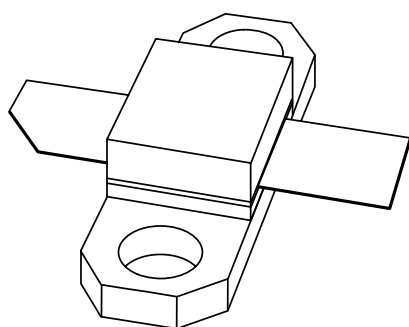


DATA SHEET



BLF2045

UHF power LDMOS transistor

Product specification
Supersedes data of 2003 Feb 27

2004 Feb 11

UHF power LDMOS transistor

BLF2045

FEATURES

- Typical 2-tone performance at a supply voltage of 26 V and I_{DQ} of 500 mA
 - Output power = 30 W (PEP)
 - Gain = 12.5 dB
 - Efficiency = 32%
 - $d_{im} = -26$ dBc.
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (1800 to 2200 MHz)
- No internal matching for broadband operation.

APPLICATIONS

- RF power amplifiers for GSM, EDGE, CDMA and W-CDMA base stations and multicarrier applications in the 1800 to 2200 MHz frequency range
- Broadcast drivers.

DESCRIPTION

30 W LDMOS power transistor for base station applications at frequencies from 1800 to 2200 MHz.

PINNING

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

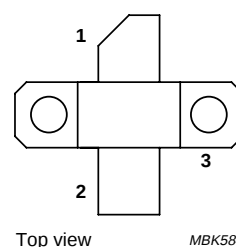


Fig.1 Simplified outline.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BLF2045	–	plastic surface mounted package; 3 leads	SOT467C

QUICK REFERENCE DATA

RF performance at $T_h = 25$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	$f_1 = 2000$; $f_2 = 2000.1$	26	30 (PEP)	>10	>30	≤ -25

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	± 15	V
I_D	drain current (DC)	–	4.5	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-h)}$	thermal resistance from junction to heatsink	$P_{tot} = 87.5\text{ W}$; $T_h = 25\text{ °C}$; note 1	2.1	K/W

Note

1. Thermal resistance is determined under specified RF operating conditions.

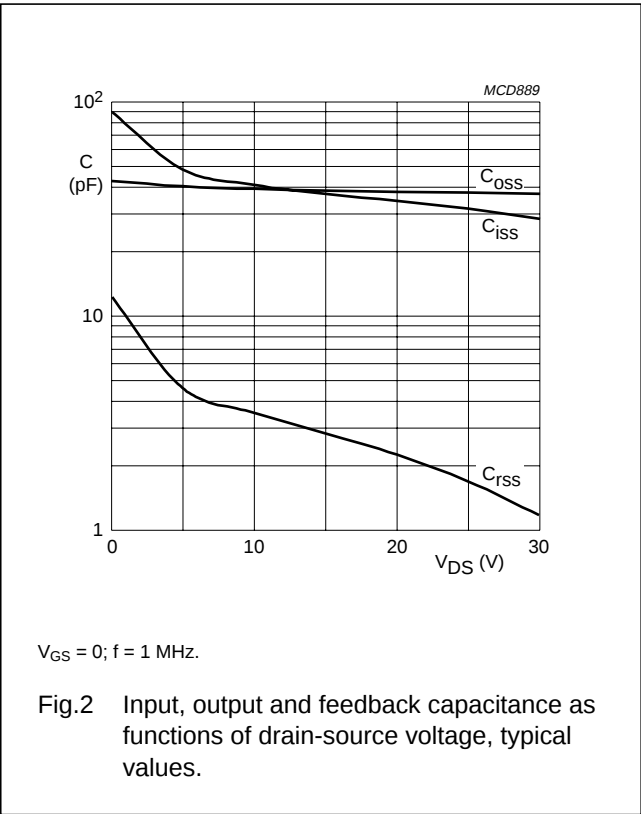
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CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0; I _D = 0.7 mA	65	–	–	V
V _{GSth}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 70 mA	1.5	–	3.5	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = 26 V	–	–	5	µA
I _{DSX}	drain cut-off current	V _{GS} = V _{GSth} + 9 V; V _{DS} = 10 V	9	–	–	A
I _{GSS}	gate leakage current	V _{GS} = ±15 V; V _{DS} = 0	–	–	125	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 2.5 A	–	2	–	S
R _{DSon}	drain-source on-state resistance	V _{GS} = V _{GSth} + 9 V; I _D = 2.5 A	–	340	–	mΩ
C _{iss}	input capacitance	V _{GS} = 0; V _{DS} = 26 V; f = 1 MHz	–	38	–	pF
C _{oss}	output capacitance	V _{GS} = 0; V _{DS} = 26 V; f = 1 MHz	–	31	–	pF
C _{rss}	feedback capacitance	V _{GS} = 0; V _{DS} = 26 V; f = 1 MHz	–	1.7	–	pF



UHF power LDMOS transistor

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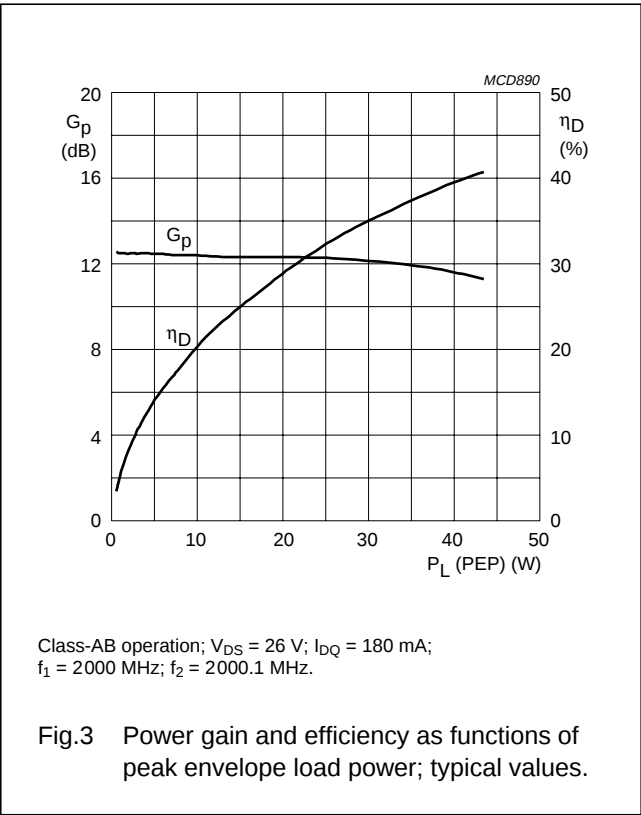
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25\text{ }^{\circ}\text{C}$; $R_{th(mb-h)} = 0.65\text{ K/W}$, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	I _{DQ} (mA)	P _L (W)	G _p (dB)	η _D (%)	d _{im} (dBc)
2-tone, class-AB	f ₁ = 2000; f ₂ = 2000.1	26	180	30 (PEP)	>10	>30	≤-25

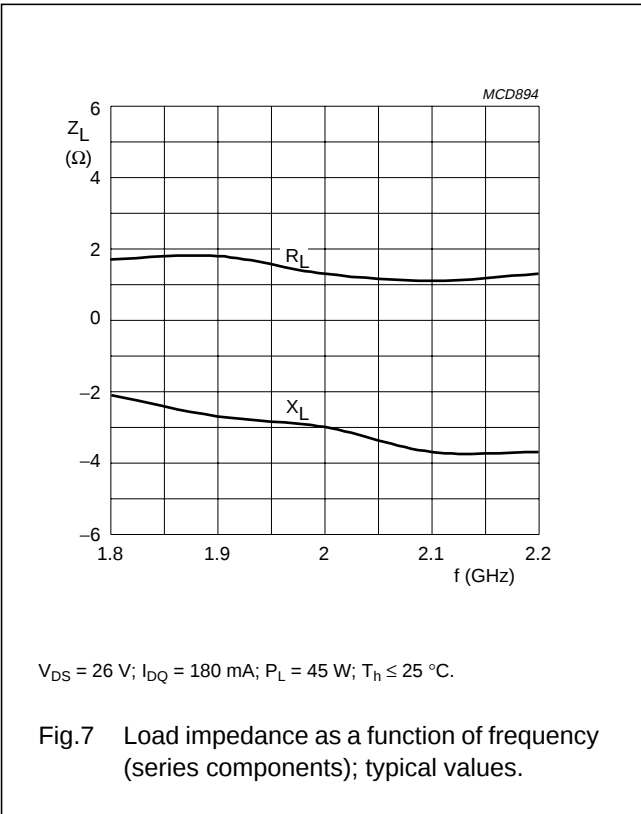
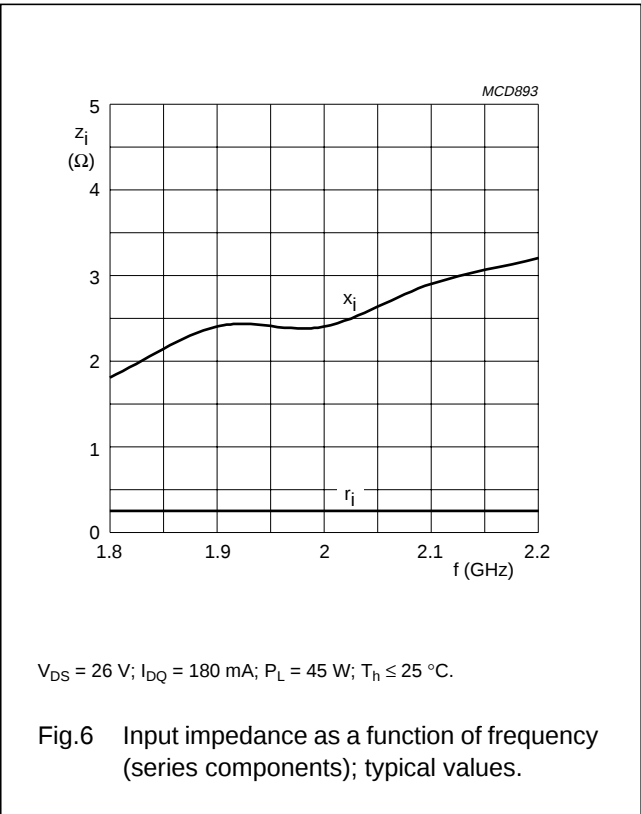
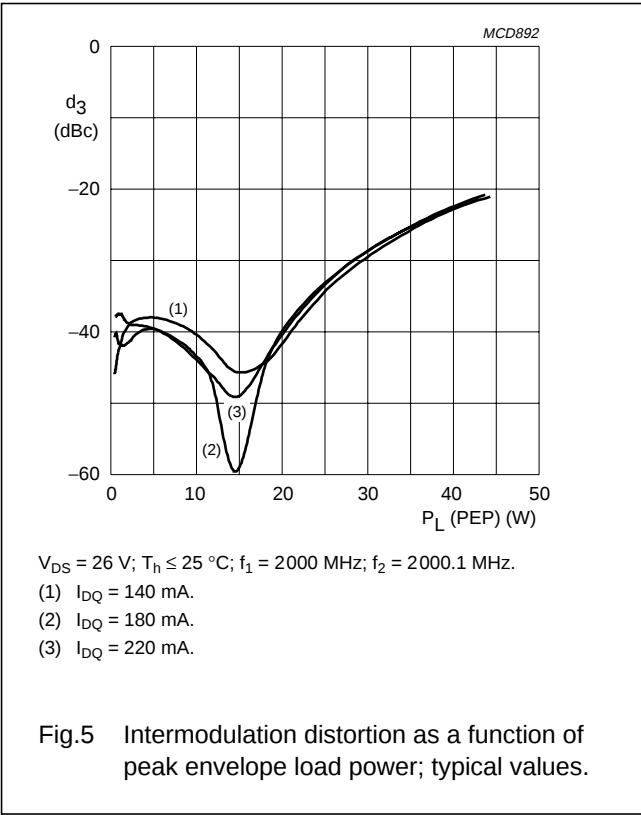
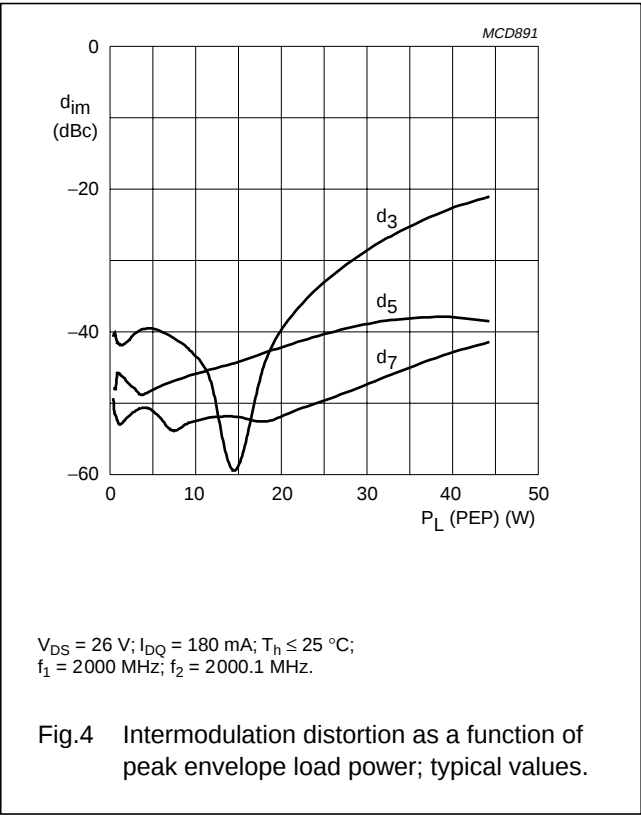
Ruggedness in class-AB operation

The BLF2045 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; P_L = 30 W (CW); f = 2000 MHz.



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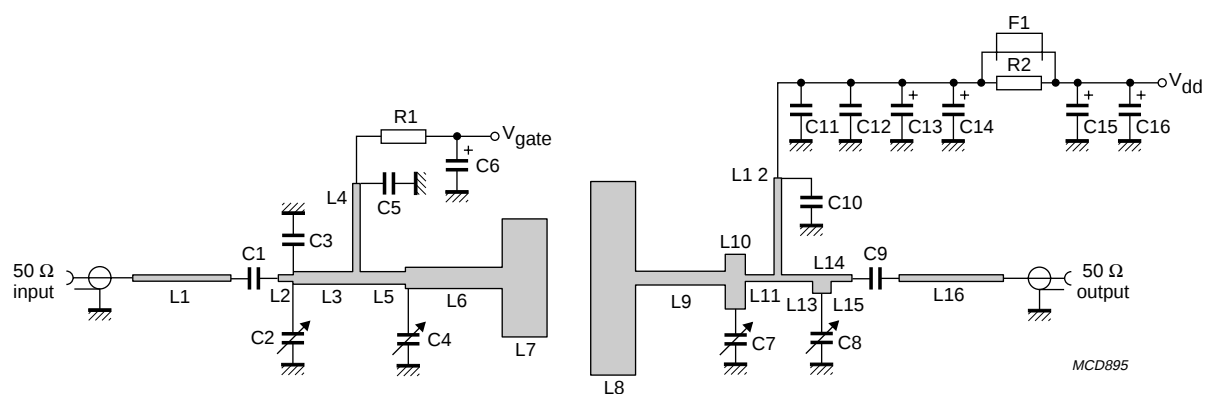


Fig.8 Class-AB test circuit for 2 GHz.

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List of components (see Figs 8 and 9)

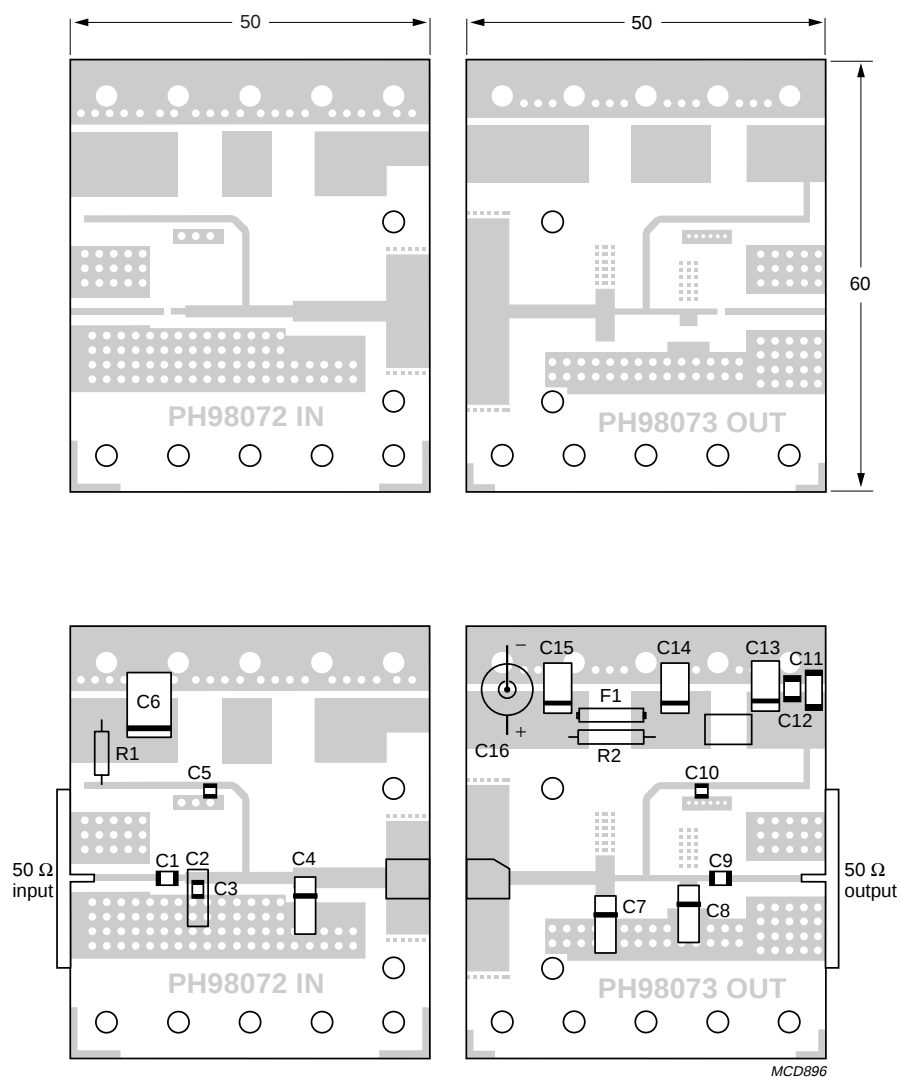
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C2, C4, C7 and C8	Tekelec variable capacitor; type 37281	0.4 to 2.5 pF		
C3	multilayer ceramic chip capacitor; note 1	2.4 pF		
C1, C5, C9 and C10	multilayer ceramic chip capacitor; note 1	11 pF		
C11	multilayer ceramic chip capacitor; note 2	1 nF		
C12	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C6, C13, C14 and C15	tantalum SMD capacitor	4.5 μ F; 50 V		
C16	electrolytic capacitor	100 μ F; 63 V		2222 037 58101
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	13 $\times$ 0.9 mm	
L2	stripline; note 3	50 Ω	2 $\times$ 0.9 mm	
L3	stripline; note 3	34.3 Ω	15 $\times$ 1.7 mm	
L4 and L12	stripline; note 3	50 Ω	37 $\times$ 0.9 mm	
L5	stripline; note 3	34.3 Ω	6 $\times$ 1.7 mm	
L6	stripline; note 3	23.6 Ω	13 $\times$ 2.9 mm	
L7	stripline; note 3	5.6 Ω	6 $\times$ 15.8 mm	
L8	stripline; note 3	3.5 Ω	6 $\times$ 26 mm	
L9	stripline; note 3	31.9 Ω	12 $\times$ 1.9 mm	
L10	stripline; note 3	24.9 Ω	7.4 $\times$ 2.7 mm	
L11	stripline; note 3	50 Ω	3 $\times$ 0.9 mm	
L13	stripline; note 3	50 Ω	4.15 $\times$ 0.9 mm	
L14	stripline; note 3	26.3 Ω	2.5 $\times$ 2.5 mm	
L15	stripline; note 3	50 Ω	2.8 $\times$ 0.9 mm	
L16	stripline; note 3	50 Ω	14 $\times$ 0.9 mm	
R1 and R2	metal film resistor	10 Ω , 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 6.15$); thickness 0.64 mm.

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Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 6.15$), thickness 0.64 mm. The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 2 GHz class-AB test circuit.

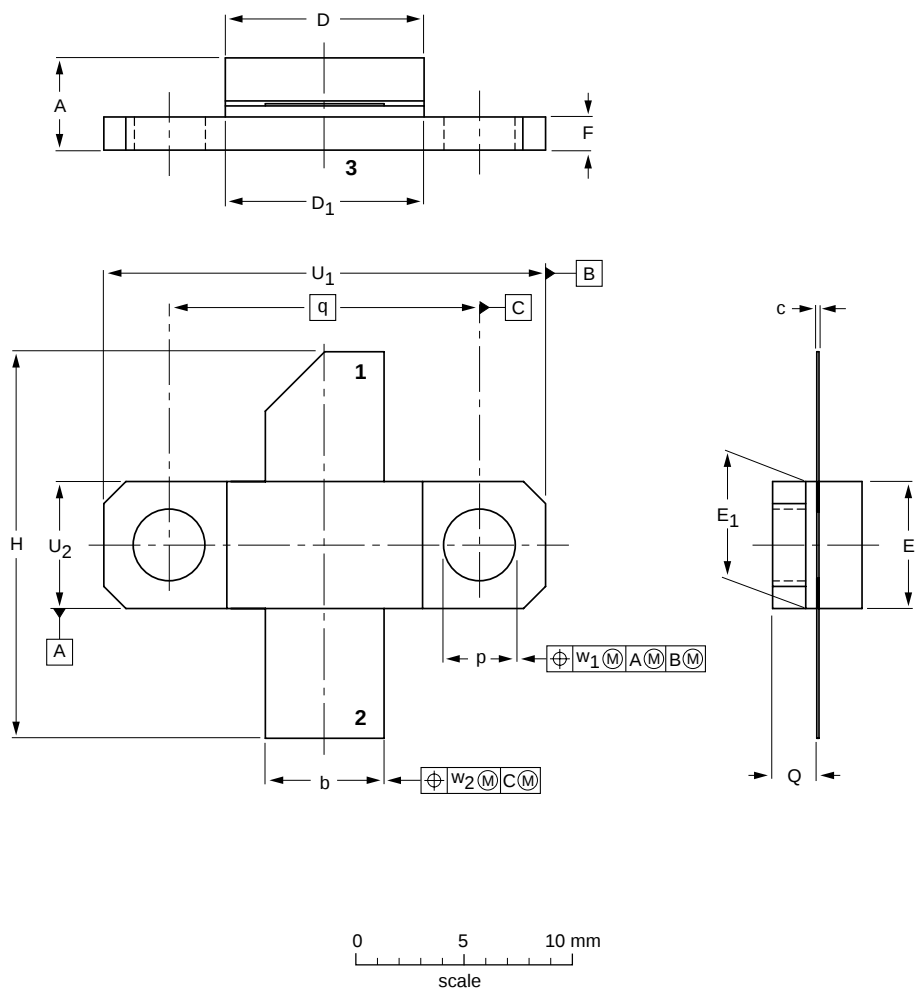
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PACKAGE OUTLINE

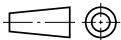
Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						99-12-06 99-12-28

UHF power LDMOS transistor

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Printed in The Netherlands

R77/06/pp12

Date of release: 2004 Feb 11

Document order number: 9397 750 12539

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